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PROVISIONAL APPLICATION FOR PATENT COVER SHEET

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No.

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Additional inventors are being named on the 2 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

MULTIPLE STACKED DIE WINDOW CSP PACKAGE AND METHOD OF MANUFACTURE

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ENCLOSED APPLICATION PARTS *(check all that apply)*

[X] Specification *Number of Pages* 5
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[ ] Application Date Sheet. See 37 CFR 1.76
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[ ] Other (specify)

METHOD OF PAYMENT OF FILING FEES FOR THIS PROVISIONAL APPLICATION FOR PATENT

[ ] Applicant claims small entity status. See 37 CFR 1.27.
[X] A check or money order is enclosed to cover the filing fees.
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[ ] Yes, the name of the U.S. Government agency and the Government contract number are:

Respectfully submitted,

SIGNATURE Reg No. 33,329

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Date 3/3/04

REGISTRATION NO. 29,027 *(if appropriate)*

Docket Number: V25014

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

PROVISIONAL APPLICATION COVER SHEET
Additional Page

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Docket Number V25014

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MULTIPLE STACKED DIE WINDOW CSP PACKAGE and METHOD OF MANUFACTURE

FIELD OF THE INVENTION

This invention relates generally to the field of semiconductor IC (Integrated Circuit) packaging and more particularly to the field of multi-chip packaging. This invention discloses a novel method of multi-chip packaging that serves to overcome present difficulties of such that involves chips of similar or identical sizes and of non-periphery multiple rows bond pad layout. Accordingly, this invention also provides for the design and process methodologies for the manufacture of this package.

BACKGROUND OF INVENTION

The rapid growth of portable electronics and wireless communications industry is pushing the electronics packaging industry's research and development efforts to come out with many breakthroughs and inventions.

One of the developments is multi-chip packaging. This is mainly driven by industry demand to package more functional silicon content into smaller form factor packages at lower cost. Packaging two or more silicon IC within the same IC package body reduces the area required and related cost on the printed circuit boards, on which the IC packages are mounted. In addition, multi-chip packaging enables close proximity and shorter electronic signal path between the chips in the package. This reduces electronic signal travel time and improves overall speed and performance.

One of the multi-chip packaging techniques is to stack silicon chip vertically to achieve smaller planar form factor (see figure 1). Interconnections between chips and the external terminals of the package can be achieved by conventional wire bonding, bumps in flip chip fashion, lead bonding or combinations of the abovementioned techniques. However, there are still presently several fundamental difficulties in chip stacking relating to stacking of chips of similar size and special bond pad layout designs.

For chips of similar sizes and their bond pads are arranged in non-periphery manner, for example in SDRAM chips where the bond pads arranged along the center-line of the chip (see figure 2), they cannot be stacked directly on each other because the bonding pads on the bottom chip would be blocked when the next chip is stacked into them. This makes connections, for example by wire bonding, out of the chip to the external terminals of the package impossible.

One of the techniques used for stacking vertically center row bond pads chips is to have the bottom chip's active surface facing the interposer substrate with a cut-out window. The bond pads of the bottom chip are connected out to the circuit of the interposer substrate through substrate window by fine wires. The top chip is stacked on the backside of the bottom chip with the active surface facing away from the interposer substrate, i.e. back to back format (refer to figure 3). To facilitate short wire bonding connections from the bond pads of the top chip to the circuitry of the substrate, some re-distribution techniques are being employed to bring the wire connections to the periphery of the top chip. This invention is patented by UTAC under US patent application number 2003/0197284.

The former invention is suitable for single row bond pads layout because when the chips active surface either facing upwards or downwards, the bond pads can be connected to either periphery sides of the chips. However, if the bond pads are arranged in 2 or more rows (see figure 2), the orientation of the bond pads of chip facing downwards and that of chip facing upwards are directly mirror image to each other. Especially in memory devices, the corresponding bond pads of similar chips must be connected to a set of common package external pins. This will result in crossing wires between the 2 rows of bond pads either for the top chip or the bottom chip.

Due to the window opening on the substrate, there is limitation in the routing of the conductive traces through the window opening. Conductive traces need to divert around the window opening if need to route from one side of the substrate another resulting in a longer electrical signal paths.

It is therefore the objective of this invention is to provide a mean to overcome the mirror image orientation of the bond pads layouts between the 2 similar chips and the routing difficulty of the substrate. This invention will still allow the die back to die back stacking arrangement.

SUMMARY OF THE INVENTION

A structure of a semiconductor package with a first substrate having a die receiving area and window opening and a plurality of conductive traces, a second substrate with a plurality of conductive traces, a first adhesive layer, a second adhesive layer, a last adhesive layer, a first semiconductor die having a plurality of bond pads and a last semiconductor die having a plurality of bond pads. The first semiconductor die, having two sides, with the electrically active side being mounted to the first substrate through the first adhesive layer within the die receiving area, is electrically coupled to the conductive traces. A second adhesive layer has its first side attached to the non-active side of the first semiconductor die. The second substrate, with having either single signal layer or multiple signal layers with at least one of the signal layers facing away from the second adhesive layer and having a die receiving area. The last semiconductor die, having two sides, has the electrically non-active side mounted to the second substrate through the last adhesive layers within the die receiving area. Signal transferring interconnects, such as wire bonding, are used for transferring electrical signals from the conductive traces to the external world and vise versa. The second substrate function as an avenue for signal paths to avoid any complication of interconnect crossing each other and to convey the signals to the ideal side of the package for easy connection to the package pins or between the bond pads of first and last die.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a sectional view of a typical stacked die multi-chip package.

Fig. 2 is a pictorial view of a 2 rows centerline bond pads layout semiconductor chip.

Fig. 3 is a sectional view of a typical 2 dies high-density package. The first and last die stacked back to back to each other. The first and last dies are similar in size and have the same bond pads layout. The bond pads are layout in single row in-line along the centerline of die. Bond pads on the last die are re-distributed to the periphery of the die.

Fig. 4 is a sectional view of a preferred embodiment of 2 die high-density package. The layout of the bond pads layout for the last die is arranged in 2 rows in-line along the centerline of die as shown in figure 2. The second substrate is sandwiched between the non-active side of the first and last die. Bond pads on the last die are re-distributed to the periphery of the die.

Fig 5 is a pictorial view of the preferred embodiment as shown and explained in Fig 4. It shows fine wires are used to connect the 2 rows bond pads of the last die to a plurality of circuitry in the re-distribution layers. Fine wires are used to connect from the re-distribution layers to the conductor traces in the second substrate. The conductor traces in the second substrate convey the signals from one side of the last die to the opposite side of the last die or any other sides of the last die. Fine wires are used again to connect from the second substrate to the first substrate. Circuitry in the first substrate will convey the signals from second substrate to the package pins. This same package pins can be connected to the corresponding or similar assignment bond pads of the first die.

Fig 6 is a sectional view of an alternative embodiment of a multiple die arrange in stacked format. The first die has bond pads layout arranged along the periphery of the die. The bond pads of last die are

arranged in periphery of the die. The conductor traces in the second substrate convey the signals from one side of the last die to the opposite side of the last die or any other sides of the last die.

Fig 7 shows an extension of fig4. Direct wire bonding from the last die to the said second substrate without any re-distribution features on the last die.

Fig 8 shows another sectional view of an alternative embodiment of a multiple die arrange in stacked format. The first die has bond pads layout arranged along the periphery of the die. The last die can be non-identical to the first die. The bond pads of last die can be arranged near or along the centerline of the die. The conductor traces in the second substrate convey the signals from one side of the last die to the opposite side of the last die or any other sides of the last die.

Fig 9 shows another sectional view of an alternative embodiment of a multiple die arrange in stacked format. A semiconductor die is flip-chip onto the second substrate. The last semiconductor die is attached to the non-active side of the flip-chip die.

Fig 10 shows another sectional view of an alternative embodiment of a multiple die arrange in stacked format. Spacer is used to separate the 2 semiconductor die whoseactive side are facing away from the package pins.

Fig 11A shows a typical conductor traces routing and its terminals using single conductor layer for the second substrate. Interconnects convey signals to/from the last die or the first substrate through the terminals along the 2 sides of the second substrate.

Fig 11B shows a typical conductor trace routing and its terminals using 2 conductor layers. Interconnects convey signals to/from the last die or the first substrate through the terminals on any sides of the second substrate.

Fig 11C shows a sectional view of a second substrate pre-prepared such that the laminate substrate or lead-frame was strengthened by adhering to a more rigid material.

Fig 12 – Method of Manufacture for the preferred embodiment shown in figure 4.

DESCRIPTION OF THE PREFERRED EMBODIMENT

To be drafted.

CLAIMS

1. A structure of a semiconductor package, said structure comprising :

A first substrate having a die receiving area, a first adhesive layer, a window opening, and a plurality of conductive traces;

A first semiconductor die, having two sides, with the electrically active side being mounted to said substrate through the first adhesive layer, within said die receiving area, for electrically coupling to said conductive traces;

A second adhesive layer having a first side attached to the non-active side of the first semiconductor die;

A second substrate having a receiving area, and a plurality of conductive traces and terminals commonly known as bond fingers;

A last adhesive layer having a first side attached to the side of the second substrate with the terminals;

A last semiconductor die, having two sides, with the electrically non-active side being mounted to the second side of the third adhesive layer; and the electrically active side being electrically coupled to said conductive traces of the said first or second substrates directly or through some re-distribution means;

An encapsulant, to encapsulate the semiconductor die and electrical coupling;

Signal transferring interconnects, for transferring an electrical signal from the said conductive traces, to the external world.

2. The first semiconductor die has a plurality of bond pads, whereby the bond pads are located within the window opening of the substrate.

3. The first semiconductor die has a plurality of bond pads, whereby the bonds pads are not located within the window opening of the substrate, and the bond pads are electrically relocated to the window opening by a redistribution means.

4. The last semiconductor die has a plurality of bond pads, whereby the bond pads are located near to the peripheral of the semiconductor die.

5. The last semiconductor die has a plurality of bond pads, whereby the bond pads are not located near the peripheral of the semiconductor die, and the bond pads are electrically relocated to the peripheral of the semiconductor die by a redistribution means.

6. The redistribution means is by wafer redistribution layer.

7. The redistribution means is by a substrate interposer with a plurality of conductive traces, attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical coupling from the bond pads to the substrate interposer.

8. The redistribution means is by a metallic interposer with a plurality of conductive traces, attached to the active surface of the last semiconductor die with an adhesive, with a plurality of electrical coupling from the bond pads to the metallic interposer.

9. The adhesive layer is an adhesive paste or coating.

10. The adhesive layer is an adhesive film.

11. The first semiconductor die size can be smaller, equal or larger than the last semiconductor die size.

12. The electrically coupling from the semiconductor die to said first substrate is by a wire bond method.

13. The electrically coupling from the semiconductor die to said first substrate is by a TAB method.

14. Direct wire bonding from the bond pads of the last die to the first or second substrate without going through any re-distribution means (figure 7 & 8).

15. The said first semiconductor die is electrically coupled to the said first substrate by a flip chip method.

16. The said last semiconductor die is electrically coupled to the said second substrate by a flip chip method.

17. The said last semiconductor die is stacked whose non-active side is facing the non-active side of a flip-chip semiconductor die. The flip-chip interconnect of the flip-chip die is on the said second substrate.

18. The said second substrate either of the following mat erials :
   a) Silicon
   b) Ceramics
   c) Laminate
   d) Aluminum
   e) Any material that can be pre-manufacture with plurality of conductor traces.

19. The said second substrate is either thin laminate or flexible circuit or lead-frame and pre-processed to make it more rigid for the later attachment and electrical interconnects process. One possible pre-processing method is by adding molding compound to the side of the substrate that is going to be face the said second adhesive layer. (See fig 11C)

20 The said second substrate having terminals along all its periphery allowing interconnects as such wire bonding to convey electrical signals to and fro between the said last semiconductor die and the said first substrate at any sides of the last semiconductor die.

21 The said second substrate with its plurality of conductive traces having the terminals positioned in an optimum locations along its periphery such that when wire bonding from these terminals locations to the first substrate allow shortest paths to the package external pins.

22 The said second substrate with its plurality of conductive traces having the terminals positioned in an optimum locations along its periphery such that when wire bonding from these terminals locations to the first substrate allow shortest paths to the interconnection from the first semiconductor die.

23. A plurality of dies are in between the first and last semiconductor die, whereby the semiconductor die between the first and the last semiconductor die are electrically coupled to the said first or second substrate.

24. The plurality of die can be smaller , equal or larger than the first or last semiconductor die.

25. Spacer is used in the stacking of the semiconductor die.

26. The window opening is a plurality of openings in the substrate coinciding with the bond pads of the first semiconductor die.

27. The encapsulant is a liquid encapsulant.

28. The encapsulant is a transfer molded molding compound.

29. The encapsulant is applied to the whole package and as well as cure at the same time.

30. The encapsulant is a lid to cover the said semiconductor die and electrical coupling.

31. All the adhesive layers can be pre-attached to the receiving side or to the respective matching side of the part going to attach to the receiving side.

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Draft for New Patent Application : Multiple Stacked Die Window CSP and Method of Manufacture

DRAWINGS

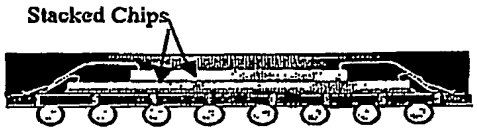

Figure 1

Figure 2

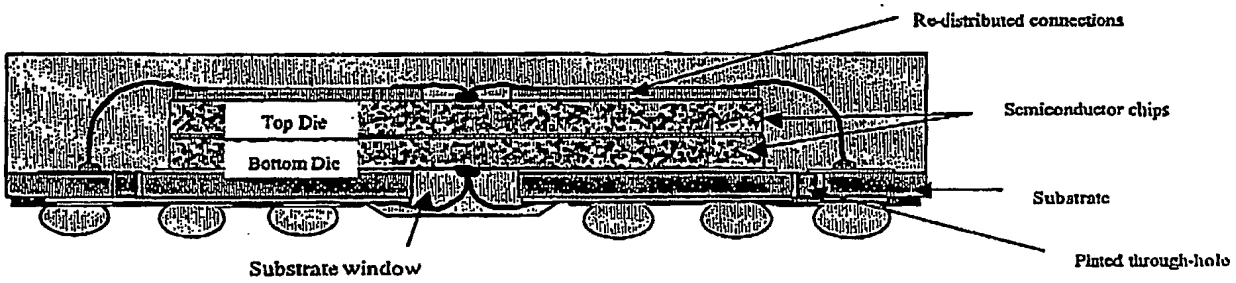

Figure 3

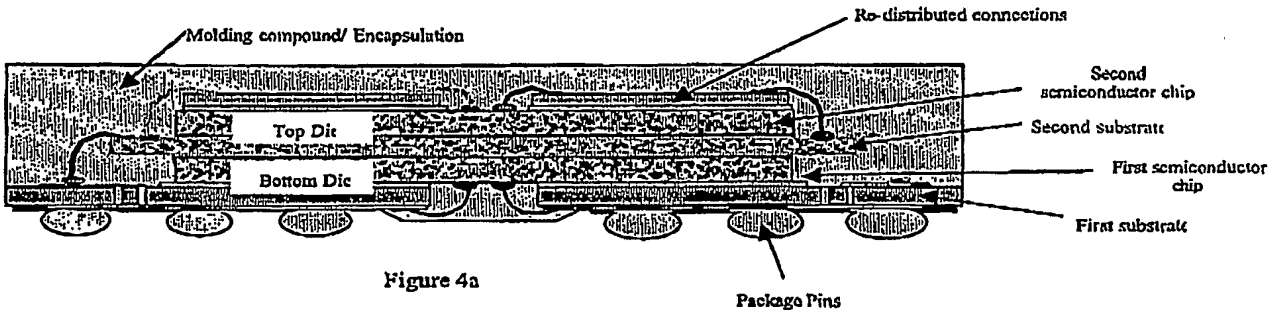

Figure 4a

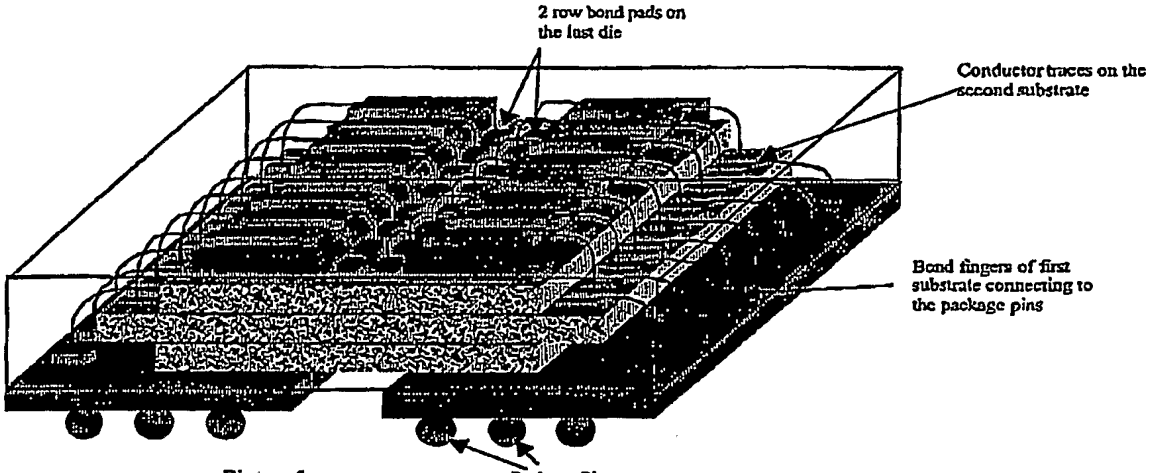

Figure 5

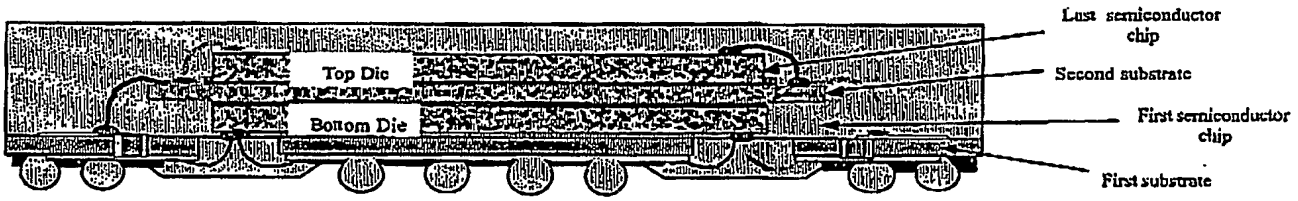

Figure 6

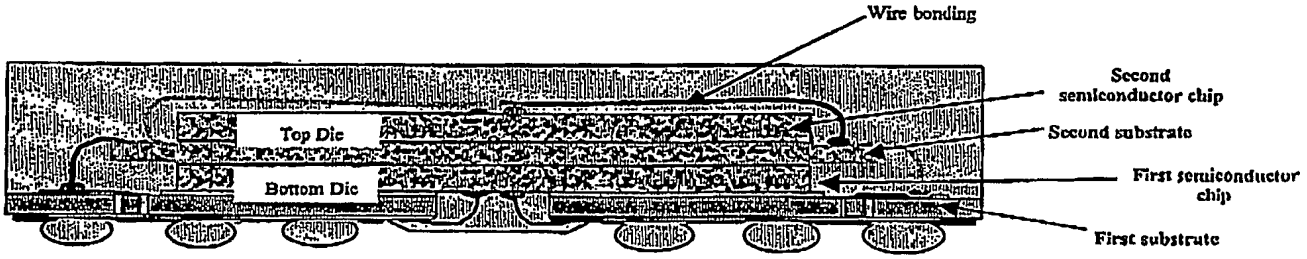

Figure 7

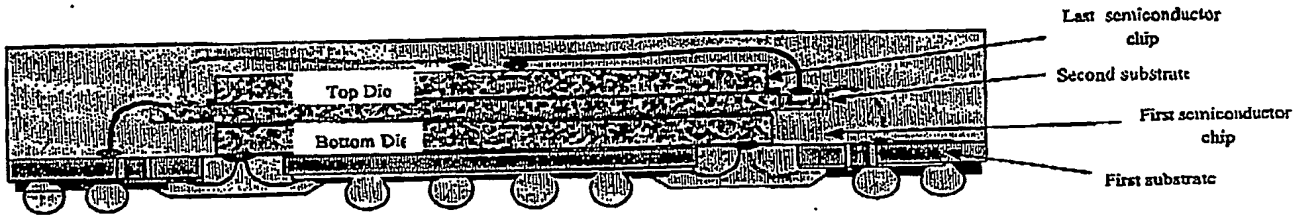

Figure 8

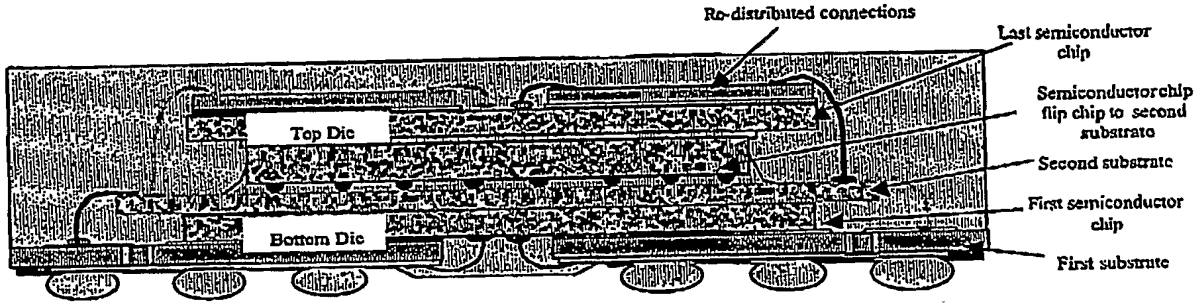

Figure 9

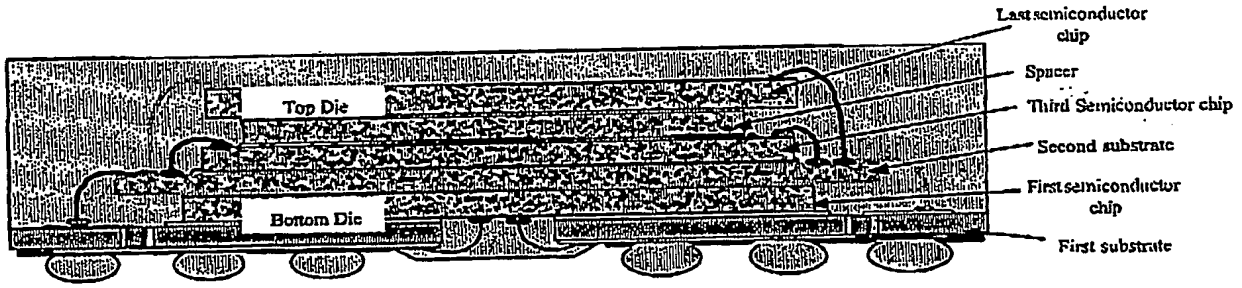

Figure 10

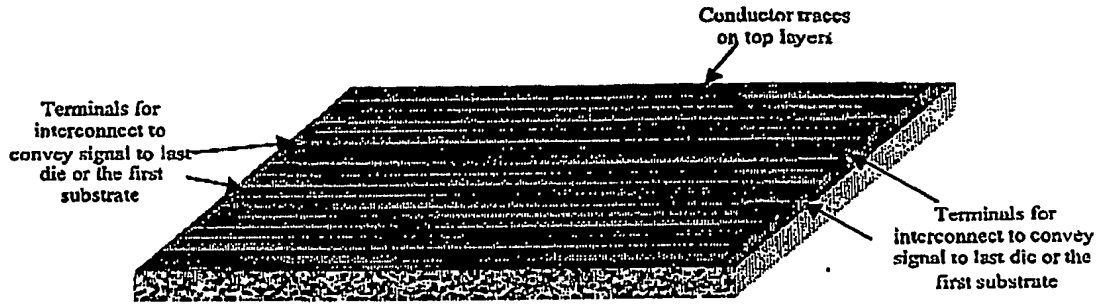

Figure 11A

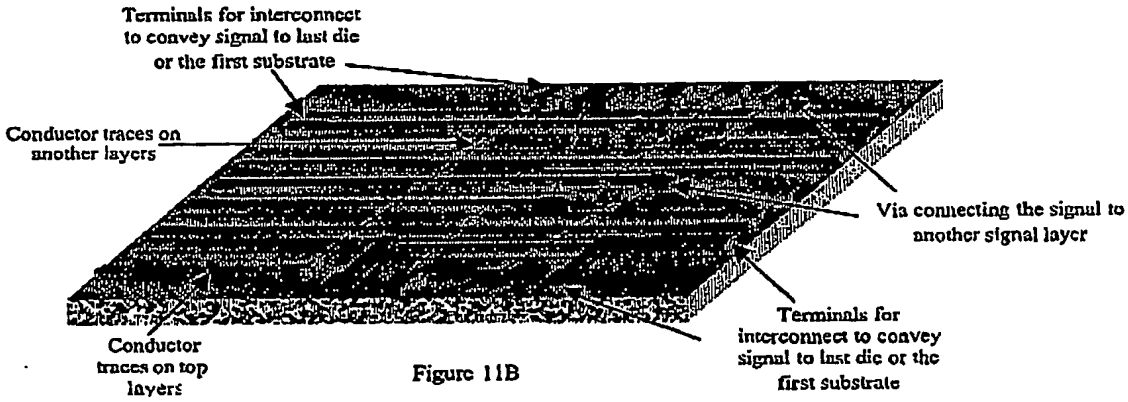

Figure 11B

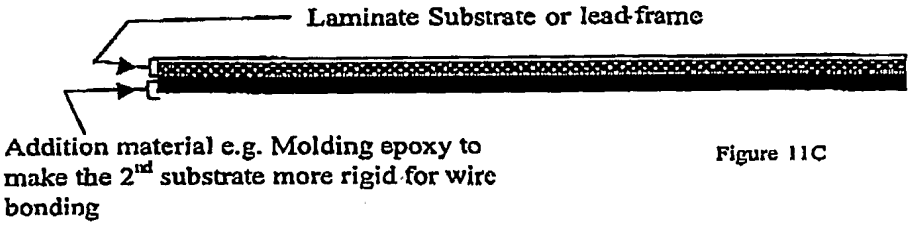

Figure 11C

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Figure 12: Method of Manufacture (1/2)

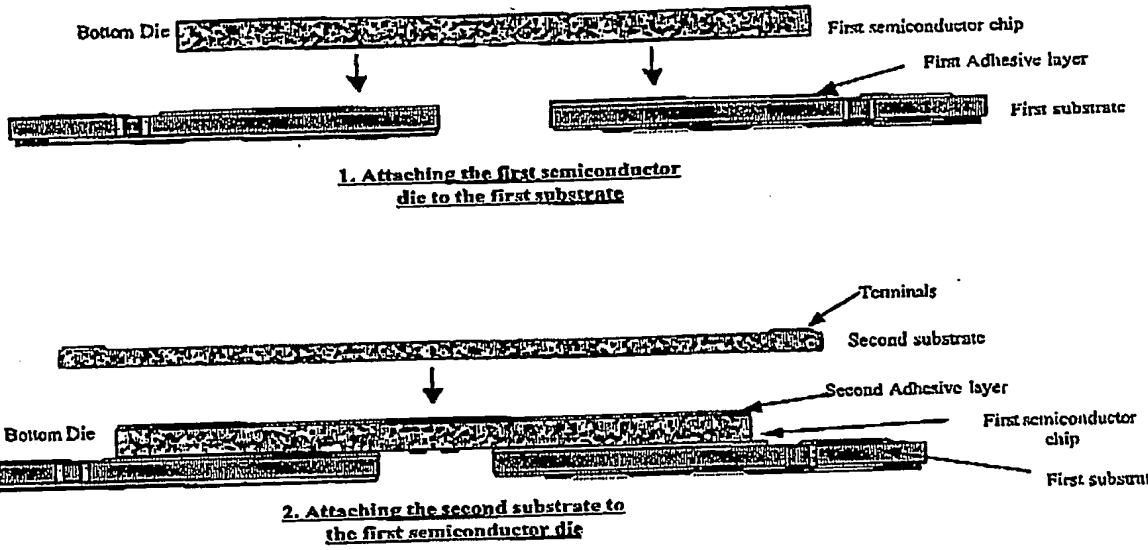
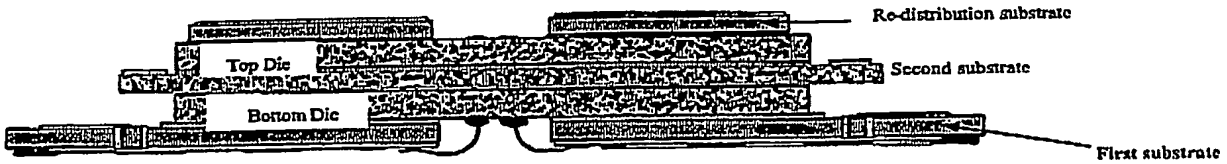
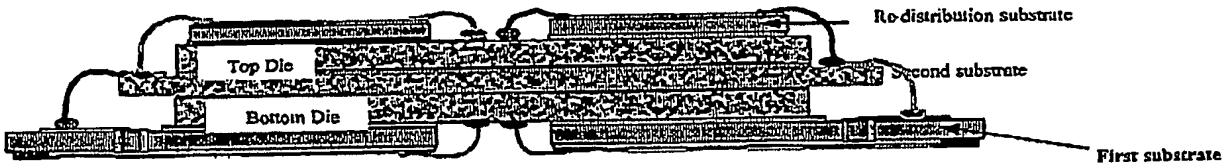


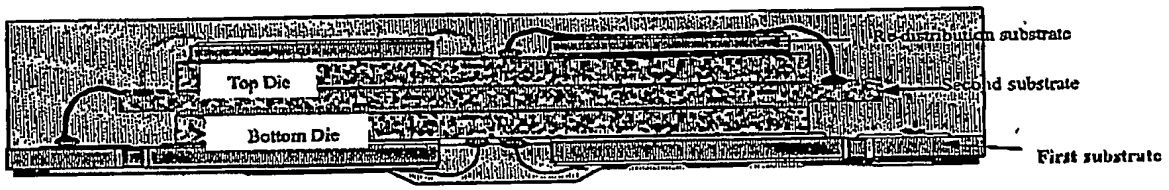
Figure 12: Method of Manufacture (2/2)



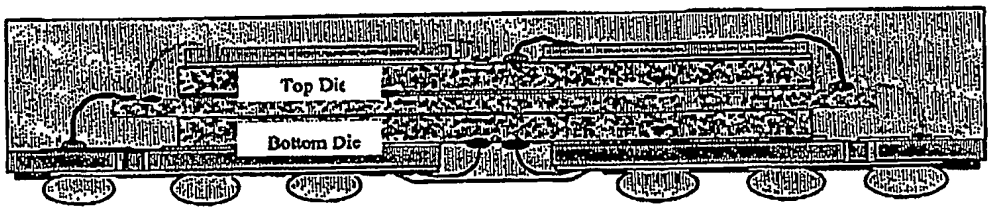
5. Wire bonding to the first semiconductor die

6. Wire bonding on the die side of the first substrate





7. Transfer molding on both the die side and solder ball side of the first substrate at the same time



8. Solder ball attach to the first substrate